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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,109	03/29/2004	James A. Mott	SUN-P8922	1538
57960 7590 01/06/2009 PVF -- SUN MICROSYSTEMS INC. C/O PARK, VAUGHAN & FLEMING LLP 2820 FIFTH STREET DAVIS, CA 95618-7759				
EXAMINER				
WONG, WARNER				
ART UNIT		PAPER NUMBER		
2416				
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/812,109

Applicant(s)

MOTT, JAMES A.

Examiner

WARNER WONG

Art Unit

2416

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 October 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1, 11, 30, 32 and 56-64 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1, 11, 30, 32 and 56-74 is/are allowed.
- 6) ☒ Claim(s) 75 and 77-84 is/are rejected.
- 7) ☒ Claim(s) 76 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 75, 77-81 and 83-84 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hendel (US 2004/0120332) In view of Pekkala (US 2002/0085493).

Regarding claim 75, Hendel describes an apparatus for flow controlling Infiniband traffic, comprising:

a single memory structure for queuing Infiniband traffic received via multiple virtual lanes and multiple queue pairs (para. 6 & 27-28, sharing the memory resource for the input traffic to the queue pair with corresponding virtual lane);

a second memory configured to store, for each of the multiple queue pairs that is active, one or more parameters associated with operation of said queue pair (para. 6, (second) memory to store context including current amount of resource allocated to the queue & minimum guarantees (queue parameters));

a resource manager configured to manage the memory structure (para. 8, 104 and fig. 7; queue's context 608 & controller 602 control the shared pool of buffers for queuing);

Hendel fails to explicitly describe:

a first module configured to facilitate the advertisement of virtual lane credits.

parameters include a maximum number of message credits:

Pekkala describes:

An apparatus configured to facilitate the advertisement of virtual lane credits (abstract, credit flow control packets for each of the VLs);

parameters include a maximum number of message credits (para. 59, configuring the FCCL 508 credit limit value field (parameter)).

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to specify using virtual lane credit advertisements as in Pekkala for for the Infiniband system of Hendel.

The motivation for combining the teachings is that it enables an Infiniband device to support all virtual lanes allowed while maintaining an acceptable level of performance in a realistic manufacturable manner (Pekkala, para. 14)

Hendel describes a system (fig. 7) which modules supporting the InfiniBand queue pairs. Hence, it inherently describes a second module configured to facilitate the advertisement of queue pair credits (the examiner cites but not used as a reference Kagan, US 2004/0017819, para. 9, where the InfiniBand specification already provides a flow control mechanism where each credit represents 1 WQE corresponding to a QP).

Regarding claim 77, Hendel and Pekkala combined describe:

memory structure comprises a set of linked lists of memory structure buffers, including one linked list for each of the multiple pairs that are active (Hendel, para. 57, each queue is maintained in a form of linked list).

Regarding claim 78, Hendel and Pekkala combiner further suggest:

the first module comprises an InfiniBand link core (Hendel, fig. 7, each of the controlling apparatus module is consider essential (core) to the Infiniband system).

Regarding claim 79, Hendel and Pekkala combiner further suggest:

second module comprises an acknowledgement generator configured to generate transport layer acknowledgements (Hendel, fig. 7 & para. 43, mux 304 forwards (generates) ACKs to other endpoints).

Regarding claim 80, Hendel and Pekkala comber further describe:

a processor interface configured to facilitate the programming of operating parameters associated with the multiple virtual lanes and multiple queue pairs (Hendel, fig. 7, mux 324 is an interface to context 608 & controller 602 (processor) which handles VLs and queue pairs).

Regarding claim 83, Hendel and Pekkala combined suggest:

a (dedicated) threshold that identifies a subset of said number of shared memory structure buffers (Pekkala, abstract, predetermined threshold for the shared transmitting buffer only (subset), not the receiving buffer).

for the (dedicated) threshold, identifying a number of message credits the queue pair may advertise when the amount of shared portion used by the multiple queue pairs exceeds said shared threshold (Pekkala, para. 19, if free space in memory drops below a predetermined threshold, flow control credits are advertised).

Regarding claim 84, Hendel and Pekkala combined suggest:

a (shared) threshold that identifies a subset of said number of shared memory structure buffers (Pekkala, abstract, predetermined threshold for the shared transmitting buffer only (subset), not the receiving buffer).

for (shared) threshold, identifying a number of message credits the queue pair may advertise when the amount of shared portion used by the multiple queue pairs exceeds said shared threshold (Pekkala, para. 19, if free space in memory drops below a predetermined threshold, flow control credits are advertised).

Allowable Subject Matter

2. Claims 1, 11, 56 and 67 allowed.

The following is an examiner's statement of reasons for allowance: the prior art fails to describe an Infiniband method comprising virtual lanes and queue pairs with first memory structure and second memory, further comprising:

"if storing the first payload in the memory structure would exceed said portion of the memory structure allocated to the first queue pair, determining whether the first queue pair is enabled to use a shared portion of the memory structure to store payloads of packets received via the first queue pair".

Claims 30 and 32 allowed.

The following is an examiner's statement of reasons for allowance: the prior art fails to describe an Infiniband method comprising virtual lanes and queue pairs with first memory structure and second memory, further comprising:

"maintaining a second memory configured to store, for each of the multiple queue pairs that is active, one or more parameters associated with operation of said queue pair, wherein said parameters include:

a maximum number of message credits advertisable by said queue pair;

a maximum number of memory structure buffers dedicated to storing payloads of packets received via said queue pair;

an indicator configured to indicate whether said queue pair is enabled to used a set of shared memory structure buffers are available for use by said queue pair to store payloads of packets received via said queue pair if:

said queue pair has used said maximum number of memory structure buffers;

and

said indicator indicates that said queue pair is enabled to use said set of shared memory structure buffers; and

a maximum number of message credits advertisable by said queue pair when said queue pair starts using said shared memory structure buffers."

Claim 72 is allowed.

The following is an examiner's statement of reasons for allowance: the prior art fails to describe an Infiniband method comprising virtual lanes and queue pairs with first memory structure and second memory, further comprising:

"identifying a first packet payload received via a first queue pair that is idle, wherein the first queue pair is considered idle if no traffic from the first queue pair is stored in said single memory structure;

for each other queue pair for which traffic from said queue pair is stored in said single memory structure, determining whether sufficient space in the single memory structure is reserved for reassembling said traffic; and

storing the first packet payload in said single memory structure only if sufficient space in the single memory structure is available for reassembling said traffic."

Claim 76 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim 76, the following is a statement of reasons for the indication of allowable subject matter: the prior art fails to describe an Infiniband method comprising virtual lanes and queue pairs with first memory structure and second memory, further comprising:

"a maximum number of memory structure buffers dedicated to storing payloads of packets received via said queue pair;

an indicator configured to indicated whether said queue pair is enabled to used a set shared memory structure buffers; and

a number of shared memory structure buffers in said set of shared memory structure buffers, wherein said shared memory structure buffers are available for use by said queue pair to store payloads of packets received via said queue pair if:

said queue pair has used said maximum number of memory structure buffers;
and

said indicator indicates that said queue pair is enabled to used said set of shared memory structure buffers; and

a maximum number of message credits advertisable by said queue pair when said queue pair starts using said shared memory structure buffers."

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Gupta (US 7,460,531) describing an Infiniband device with use of virtual lanes and queue pairs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to WARNER WONG whose telephone number is (571) 272-8197. The examiner can normally be reached on 6:30AM - 3:00PM, M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on (571) 272-3179. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Warner Wong
Examiner
Art Unit 2416

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Examiner, Art Unit 2416

/Chi H Pham/
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